

*U.S. Patent Application Serial No. 10/775,216
Reply to OA dated October 19, 2007*

REMARKS

Claims 1 - 28 have been canceled without prejudice or disclaimer. Claims 29 - 38 are currently pending in this patent application, claims 29, 33, 35 and 36 being independent claims.

The amendment adding synchronous oscillation of the master and slave is supported at page 16, lines 5-7. The term "simultaneously shut down" in the claims is supported by "simultaneous shutdown," which appears in the Abstract and in the last paragraphs of the Summary and Detailed Description.

In response to the Office Action dated October 19, 2007:

The applicants respectfully request reconsideration of these rejections: (1) claims 29 - 34, 36 and 38 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tominaga (U.S. Patent No. 5,237,208); and (2) claims 29-32, 35 and 37 stand rejected under 35 U.S.C. 103(a) based on Tominaga in view of Luo (U.S. Patent Publication No. 2005/0073783). The rejections are respectfully traversed. The Examiner is invited to consider:

(1) The Examiner states at page 2, lines 3-6 of ¶ 1, that "or" is interpreted as an exclusive "or" rather than a logical "or," and applies this interpretation to support the rejection. With respect, the Examiner's interpretation is contrary to the true meaning. The word "or" is often used informally with mutually exclusive conditions (such as "either it is or it isn't") but in such cases both conditions *cannot* occur. When "or" is used with *non*-exclusive conditions (as in "If either I get a raise or my rent goes down, I'll go on vacation") then the result follows from either one of the conditions *or both* ("I got a raise *and* my rent went down—I'm going on vacation!") The Examiner is invited to consider the "or" of formal logic, and the digital OR truth table.

- 11 -

*U.S. Patent Application Serial No. 10/775,216
Reply to OA dated October 19, 2007*

(2) Tominaga discloses a plurality of triport uninterruptible power source devices connected in parallel to supply an AC power all to the same load, wherein each of the plurality of triport uninterruptible power source devices inputs an AC power from an AC power source. The AC power source is supplied to the load via a triport trance transformer when the AC power source is in a normal condition. The output of an inverter is supplied to the load via the triport transformer when the AC power source is out (e.g., during a blackout), connecting in parallel an interruptible power source device which has a feature of providing outputs of the inverter to load via a triport trance to provide the power source to the same load when the AC power source is out.

On the other hand, according to the Applicants a plurality of multiple output power source apparatuses are connected in parallel configuration in which each of the plurality of multiple output power source apparatuses inputs an output voltage from a DC power source, connecting in parallel a plurality of power source circuits which raises or lowers the output voltage of the DC power source to output different DC voltages respectively to obtain a plurality of output voltages. Accordingly, the basic configuration is different.

(3) Tominaga describes a configuration in which, when an inverter 26 of any triport UPS becomes abnormal in the course of the normal mode of parallel operation (when all the triport UPS's are supplying the AC power source to the same load via the triport transformer), the inverter switch 24 and the switch 25 are opened making a parallel operation connection to release the triport UPS from the parallel operation.

*U.S. Patent Application Serial No. 10/775,216
Reply to OA dated October 19, 2007*

The Applicants describe a configuration in which, when an abnormality occurs in one of a plurality of source circuits connected by HLT terminals, it results in concurrently shutting down the plurality of power source circuits connected by the HLT terminals. Accordingly, the present invention is totally different from Tominaga in configuration and purpose.

(4) Tominaga describes a configuration in which, during the an inverter mode operation, oscillating circuit trigger pulse phases in all of the triport UPS's are made coincident to each other by the parallel synchronizing signal generating circuit 41, to substantially nullify any deviation of synchronization error among the inverters or any difference in phase among the output voltages. Therefore the circulating current is minimized by conforming the phases of the oscillating circuit trigger pulses in all of the triport UPS's by the parallel synchronizing signal generating circuit.

On the other hand, the Applicants describe a configuration in which synchronous oscillations are conducted between power source circuits connected by CLK terminals for the purpose of optimizing the efficiency by setting the optimum oscillating frequency for each output voltage, both to optimize efficiency and for the purpose of suppressing the generation of beat noise, etc. According, the present invention is totally different from Tominaga in configuration and purpose.

Luo merely describes a configuration exchanging information via a communication line 23 in a configuration connecting in parallel with a plurality of UPS modules (10)-(10N) connected in parallel.

Therefore, no combination (not admitted) could reach the instant claims.

U.S. Patent Application Serial No. 10/775,216
Reply to OA dated October 19, 2007

In view of the aforementioned amendments and accompanying remarks, the claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to **Deposit Account No. 01-2340.**

Respectfully submitted,

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I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office (Fax No. (571-273-8300) on January 14, 2008.

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Signature 